REV	00

高展工业智能显示科技有限公司

IIDWay Technology Co. Ltd

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APPROVAL SHEET

PRODUCT MODEL	**GZ70205-DIT050XG**		
REMARKS	**TFT MODULE, 768(RGB) * 1024 PIXELS**		
APPROVED SIGNATURE BY CUSTOMER	**PROJECT**	**QUALITY**	**APPROVED**

PREPARED BY	CHECKED BY	APPROVED BY

RECORDS OF REVISION

REV.	DATE	PAGE	DESCRIPTION OF CHANGES
00	2022.01.25		First issue.

CONTENT

1. GENERAL SPECIFICATION

1.1 Description

The GZ70205-DIT050XG is a color active matrix Thin Film Transistor (TFT) Liquid Crystal Display (LCD) that uses amorphous silicon(a-Si) TFT as a switching device. This model is composed of a single 7.0 inches transmissive type main TFT-LCD panel. The resolution of the panel is 1200RGBx1920 pixels and can display up to 16.2M color.

1.2 Feature

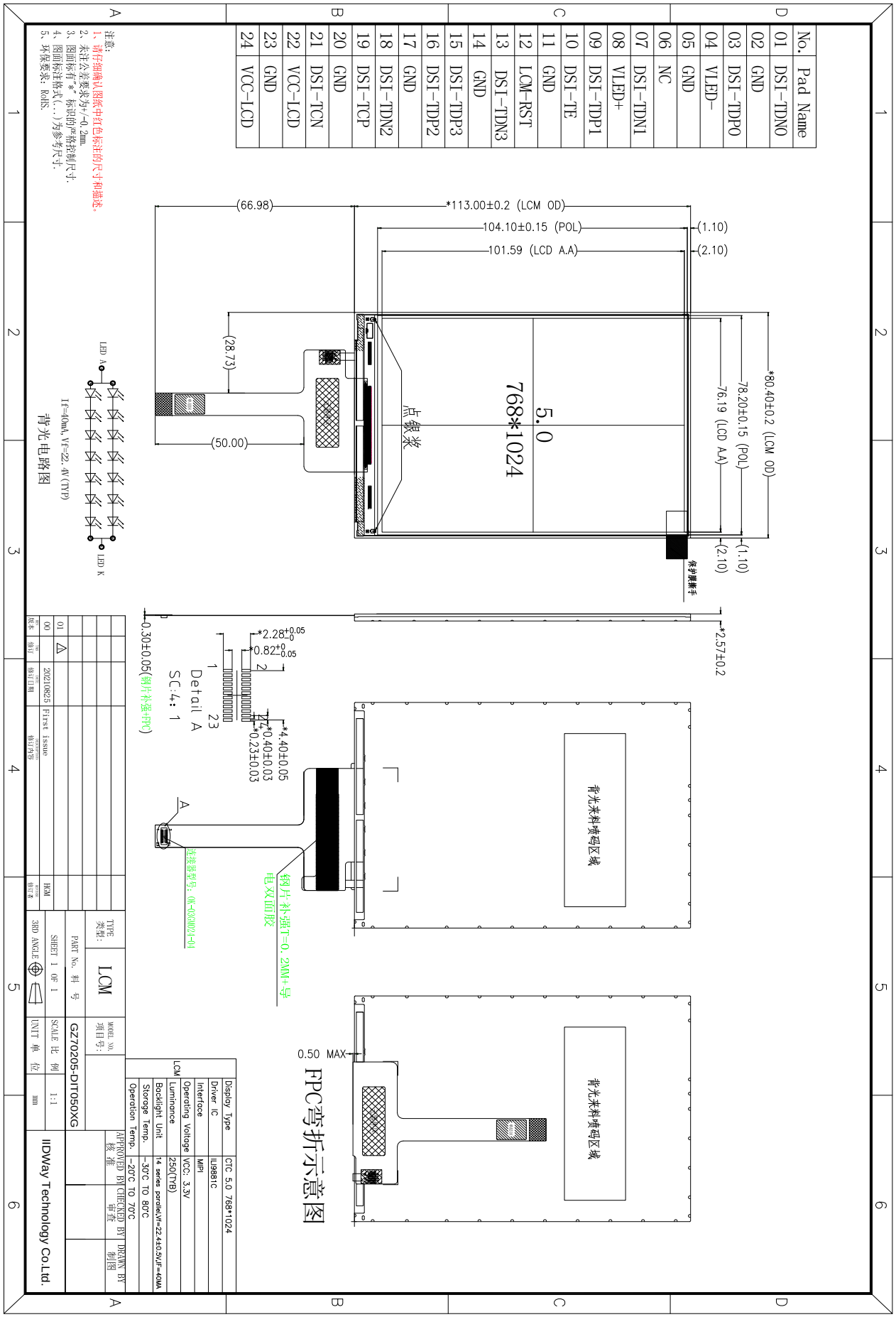
-IPS type for main TFT-LCD panel
-Structure COG+FPC
-Full, Normal (Still), Partial, Sleep mode are available

1.3 General Specification

No.	Item	Specification	Unit	Remark
1	LCD Size	5.0	inch	-
2	Panel Type	a-Si TFT active matrix	-	-
3	Resolution	768 x (RGB) x 1024	pixel	-
4	Display Mode	Normally Black,Transmissive	-	-
5	Display Number of Colors	16.2M	-	-
6	Viewing Direction	Free	-	Note
7	Contrast Ratio	1200(TYP)	-	-
8	Luminance	250	cd/m^2	-
9	Module Size	80.4(W) x113(L) x2.57(T)	mm	Note
10	Active Area	76.19(W) x 101.59(L)	mm	Note
11	Pixel Pitch	0.09921(W) x 0.09921（L）	mm	-
12	Driver IC	ILI9881C	-	-
13	Light Source	14LEDs White	-	-
14	Interface	MIPI	-	-
15	Operating Temperature	-20~70	℃	-
16	Storage Temperature	-30~80	℃	-

Note: Please refer to the mechanical drawing.

2. MECHANICAL DRAWING .

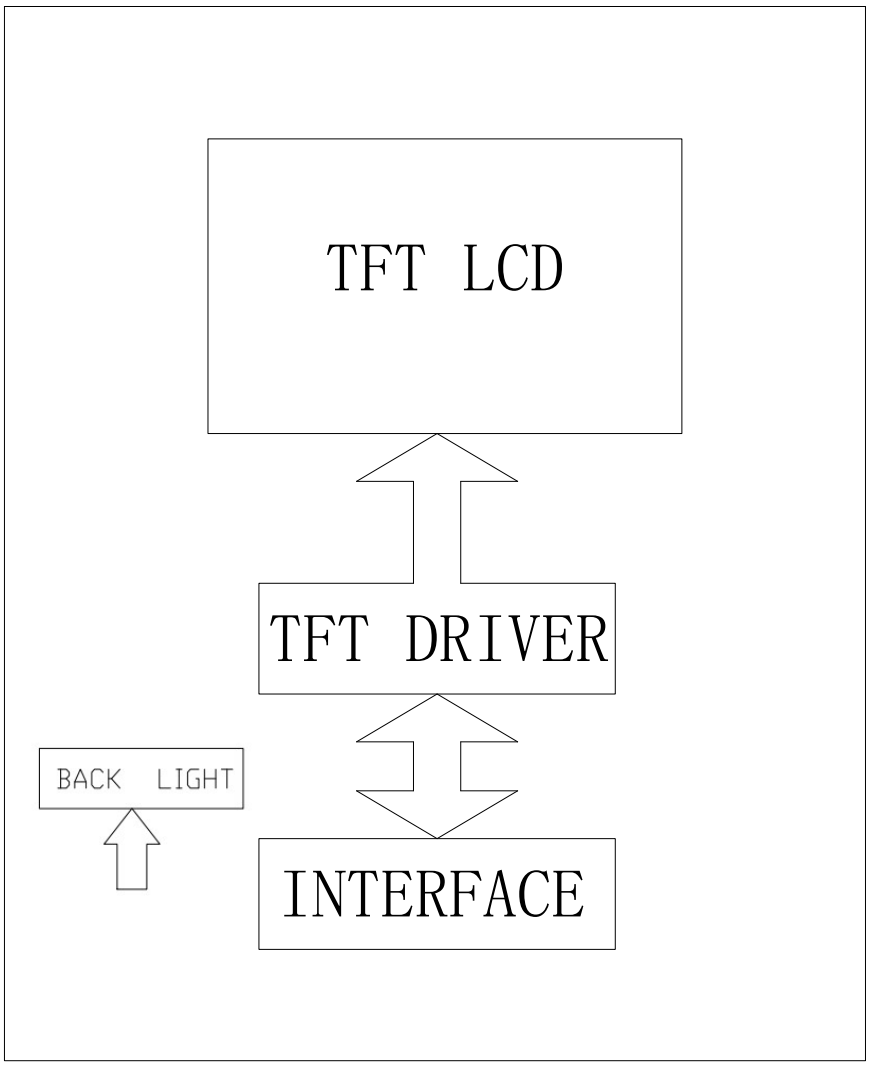


3. INTERFACE ASSIGNMENT

1	DSI-TDN0	MIPI DSI : Data differential signal input pins.
2	GND	Ground
3	DSI-TDP0	MIPI DSI : Data differential signal input pins.
4	VLED-	Cathodic power supply for backlight (LED-).
5	GND	Ground
6	NC	No connection
7	DSI-TDN1	MIPI DSI : Data differential signal input pins.
8	VLED+	Anode power supply for backlight (LED+).
9	DSI-TDP1	MIPI DSI : Data differential signal input pins.
10	DSI-TE	Tearing effect output
11	GND	Ground
12	LCM-RST	Global reset pin
13	DSI-TDN3	MIPI DSI : Data differential signal input pins.
14	GND	Ground
15	DSI-TDP3	MIPI DSI : clock differential signal input pins.
16	DSI-TDP2	MIPI DSI : clock differential signal input pins.
17	GND	Ground
18	DSI-TDN2	MIPI DSI : Data differential signal input pins.
19	DSI-TCP	MIPI DSI : clock differential signal input pins.
20	GND	Ground
21	DSI-TCN	MIPI DSI : clock differential signal input pins.
22	VCC-LCD	POWER supply for system
23	GND	Ground
24	VCC-LCD	POWER supply for system

4. ELECTRICAL SPECIFICATION

4.1. Block Diagram



4.2. Tft Absolute Maximum Ratings

ITEM	SYMBOL	CONDITION	STANDARD VALUE			UNIT
			MIN	TYP	MAX	
Power Supply for Analog	VCC-LCD	Ta=25 ºC	-0.3	-	3.6	V

Note: Permanent damage to the device may occur if maximum values are exceeded or reverse voltage is applied.

4.3. Tft Typical Operation Condition

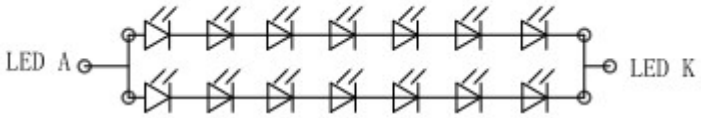
4.3.1 TFT DC Characteristics

ITEM	SYMBOL	CONDITION	STANDARD VALUE			UNIT
			MIN	TYP	MAX	
Power Supply for Analog	VCC-LCD	Ta=25 ºC	2.85	3.3	3.6	V
Input Signal “H” Level	V_{IH}	-	0.7IOVCC	-	IOVCC	V
Input Signal “L” Level	V_{IL}	-	0	-	0.3IOVCC	V
Output Signal “H” Level	V_{OH}	I_{OH}=-1.0mA	0.8IOVCC	-	IOVCC	V
Output Signal “L” Level	V_{OL}	I_{OL}=1.0mA	0	-	0.2IOVCC	V
Frame Frequency	FRAME	-	50	60	80	Hz

Note: To prevent IC latch up or DC operation in LCD panel, the power on/off sequence should follow the driver IC specification.

4.4. Backlight Specification

4.4.1 Backlight Circuit



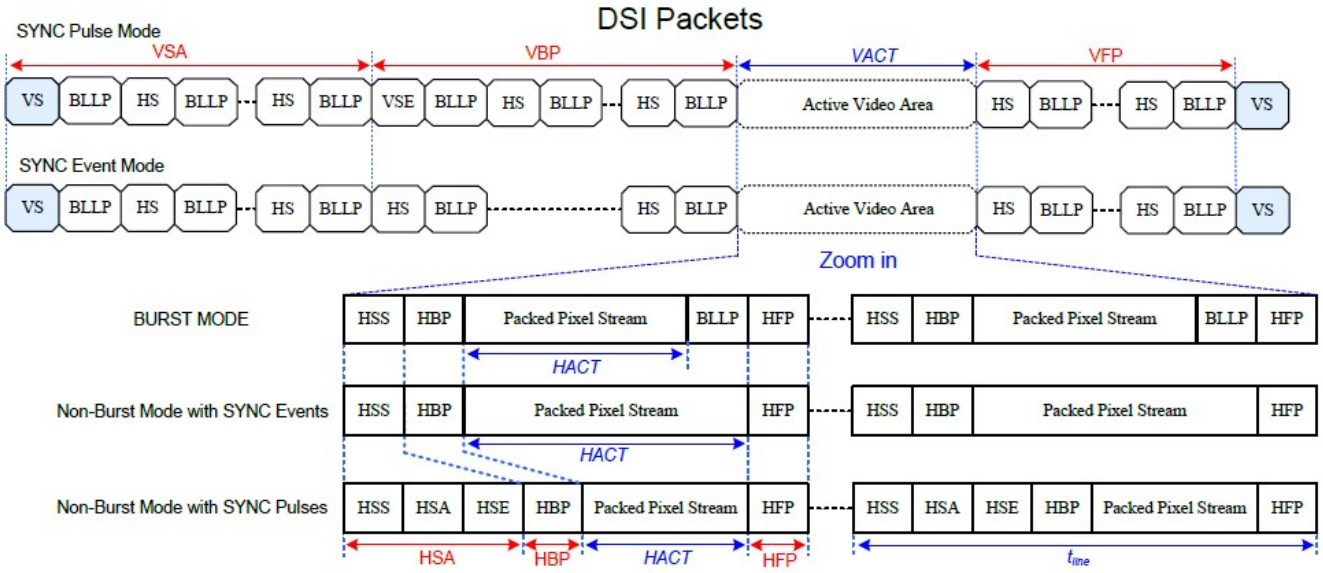
If=40mA, Vf=22.4V(TYP)

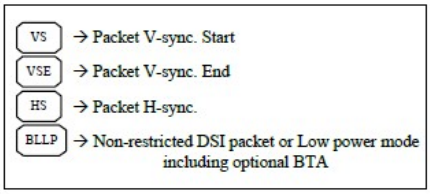
背光电路图

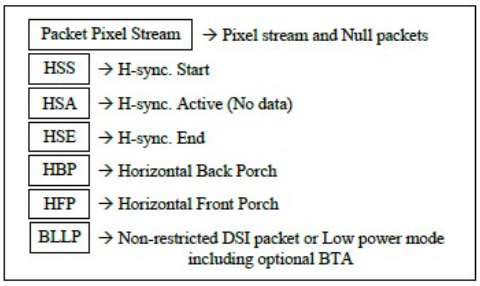
4.4.2 ELECTRICAL CHARACTERISTICS **(T=25℃)**

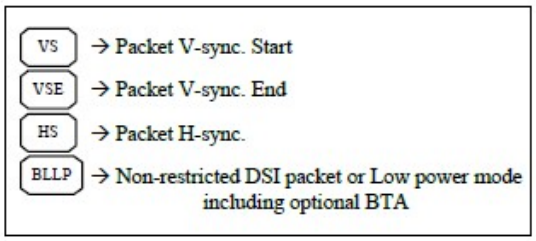
PARAMETER	SYMBOL	CONDITION	STANDARD VALUE			UNIT
			MIN	TYPE	MAX	
FORWARD VOLTAGE	VF	IF=40MA	19.6	22.4	13.8	V

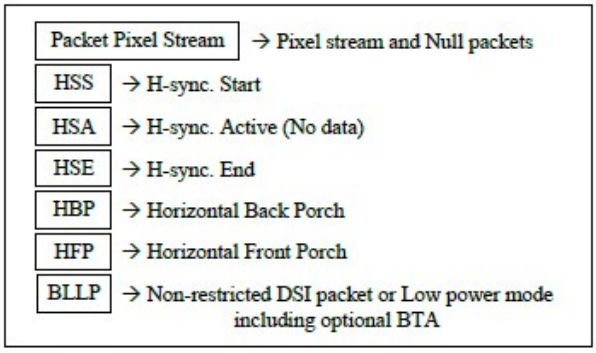
4.5.Timings for DSI Video mode:











Parameters	Symbols	Min.	Typ.	Max.	Units
Vertical sync. active	VSA	2 (Note 6)	-	-	Line
Vertical Back Porch	VBP	14 (Note 6)	-	-	Line
Vertical Front Porch	VFP	8 (Note 6)	-	-	Line
Active lines per frame	VACT	-	1280	-	Line
Horizontal sync. active	HSA	2	-	-	Pixel
Horizontal Porch period	HSA + HBP + HFP	1.6	-	-	us
Active pixels per line	HACT	-	720	-	Pixel
Bit rate	BR_{bps}	385		Note 5	Mbps/lane

1 UI=1/Bit rate

HSA(pixel)= (tHSA*lane number) / (UI* pixel format)

HBP(pixel)= (tHBP*lane number) / (UI* pixel format)

HFP(pixel)= (tHFP*lane number) / (UI* pixel format)

$$\text{Frame Rate} = \frac{BR_{bps} \times Lane_{num}}{(VACT+VSA+VBP+VFP) \times (HACT+HSA+HBP+HFP) \times \text{Pixel Format}}$$

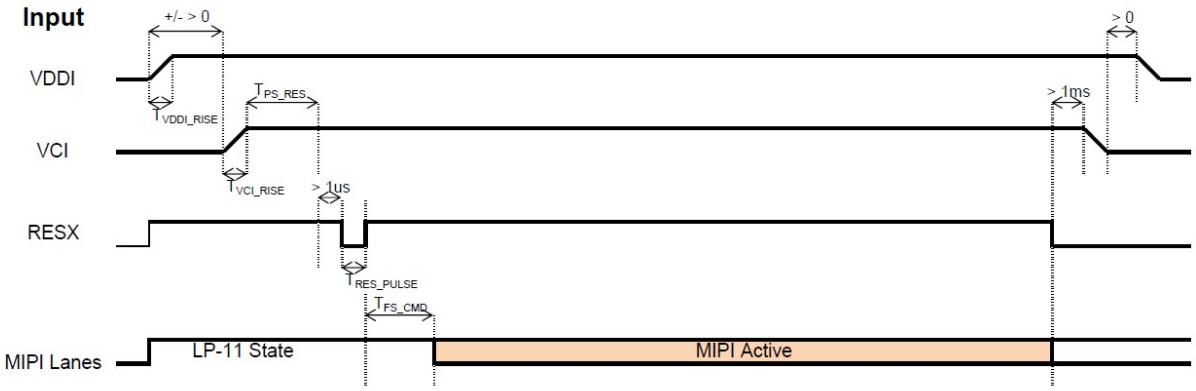
Example：BR_{bps} = 457Mbps/lane, 1UI=2.1883ns, Frame rate=60Hz, VACT=1280, VSA=2, VBP=30, VFP=20, HACT=720, HSA=33, HBP=100, HFP=100, $Lane_{num}$=4(lane), Pixel Format=24(bit).

Note:

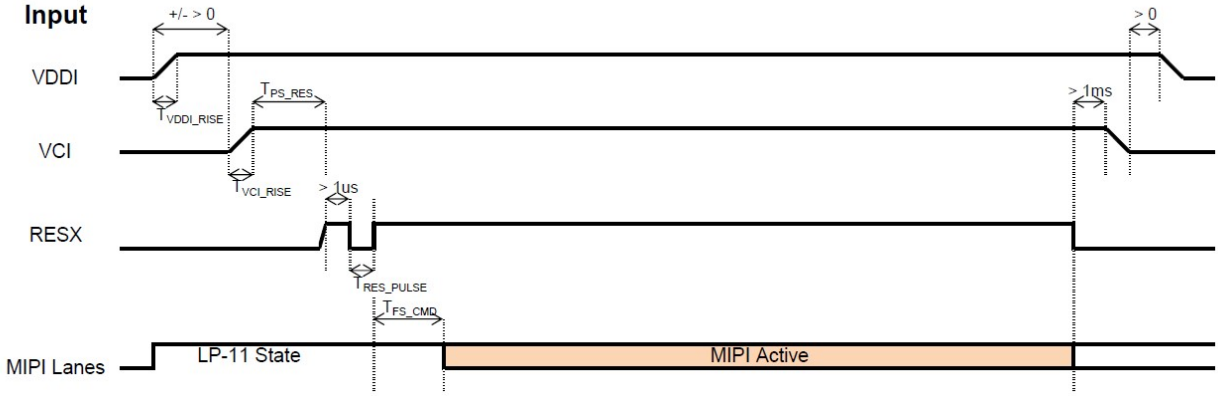
1. $Lane_{num}$: Date lane of MIPI-DSI.
2. Pixel Format: Please reference to “4.1DSI System Interface”.
3. The formula exists slightly error because of the host-transmission way.
4. The best frame rate setting： 2 data lanes：50~60 Hz / 3 data lanes：50~70 Hz / 4 data lanes：50~70 Hz.
5. Please reference to “Table 39: Limited Clock Channel Speed”.
6. The minimum values of this table mean the limitation of IC without considering the panel GIP. The actual values of VSA, VBP and VFP will be changed by different panel GIP setting.

4.6 Power On/ OFF Sequence

Case A:



Case B:



Symbol	Characteristics	Min.	Typ.	Max.	Units
T_{VDDI_RISE}	VDDI Rise time	10	-	-	us
T_{VCI_RISE}	Case A: VCI Rise time	130	-	-	us
	Case B: VCI Rise time	40			
T_{PS_RES}	VDDI/VCI on to Reset high	5	-	-	ms
T_{RES_PULSE}	Reset low pulse time	10	-	-	us
T_{FS_CMD}	Reset to first command	10	-	-	ms

4.7 Reset Input Timing:

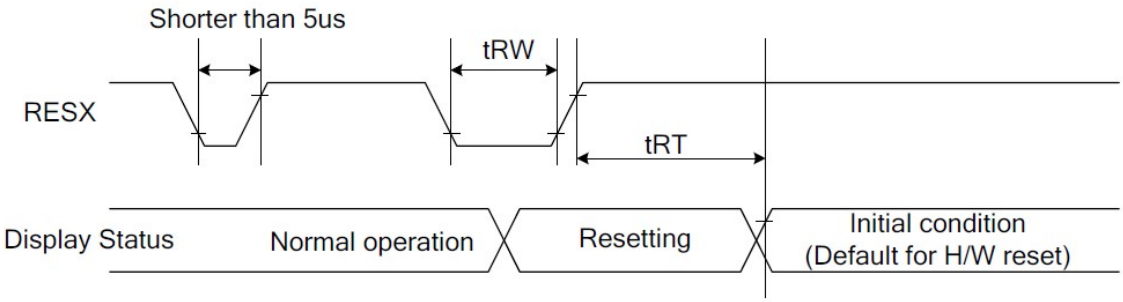


Figure 113: Reset Timing

Table 47: Reset Timing

Signal	Symbol	Parameter	Min	Max	Unit
RESX	tRW	Reset pulse duration	10		uS
	tRT	Reset cancel		5 (note 1,5)	mS
				120 (note 1,6,7)	mS

Notes:

1. *The reset cancel also includes required time for loading ID bytes, VCOM setting and other settings from EEPROM to registers. This loading is done every time when there is H/W reset cancel time (tRT) within 5 ms after a rising edge of RESX.*
2. *Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the Table 48.*

Table 48: Reset Descript

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 10us	Reset
Between 5us and 10us	Reset starts

3. During the Resetting period, the display will be blanked (The display enters the blanking sequence, which maximum time is 120 ms, when Reset Starts in the Sleep Out mode. The display remains the blank state in the Sleep In mode.) and then return to Default condition for Hardware Reset.
4. Spike Rejection can also be applied during a valid reset pulse, as shown below:

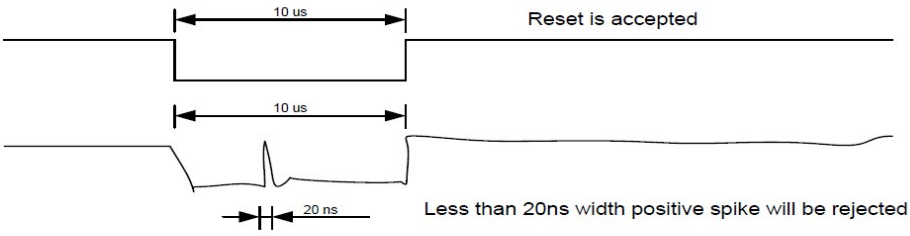


Figure 114: Positive Noise Pulse during Reset Low

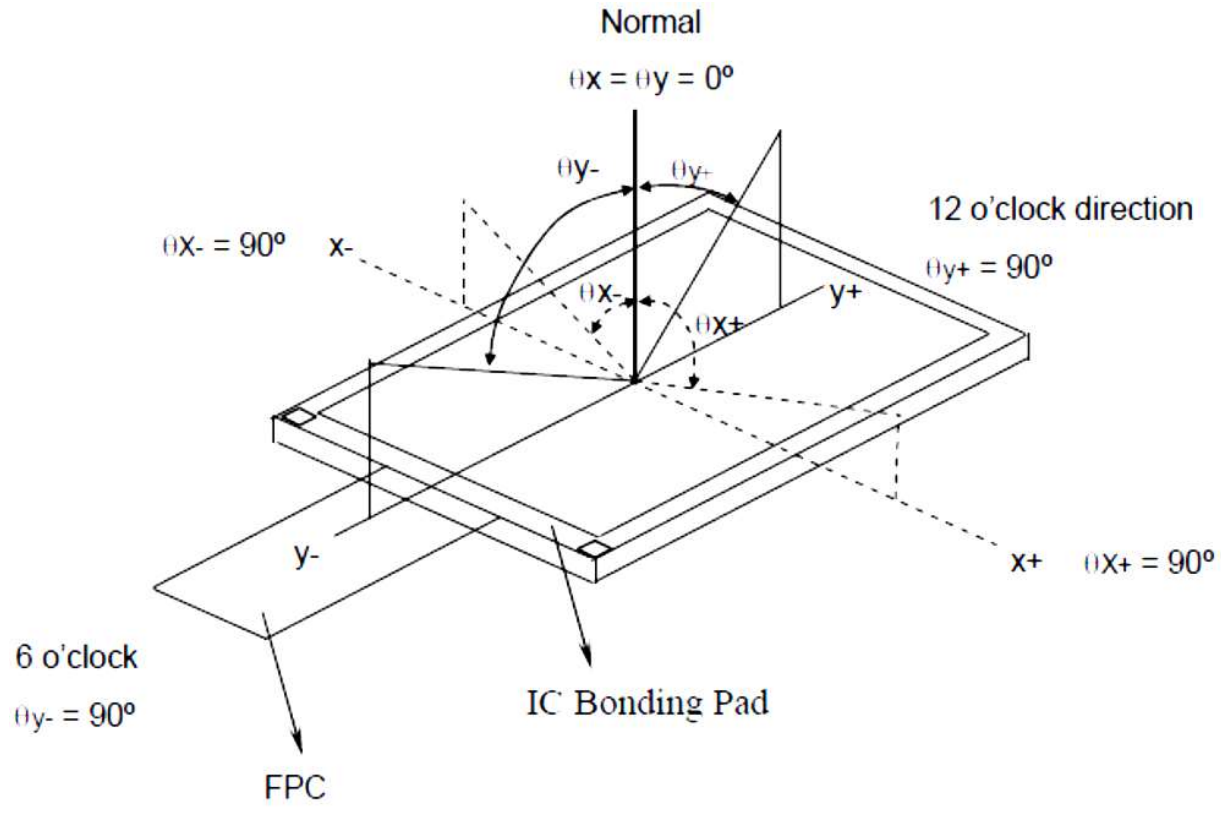
5. When Reset applied during Sleep In Mode.
6. When Reset applied during Sleep Out Mode.
7. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

5. LCD OPTICAL CHARACTERISTICS

(T_a=+25ºC, IOVCC=+1.8V)

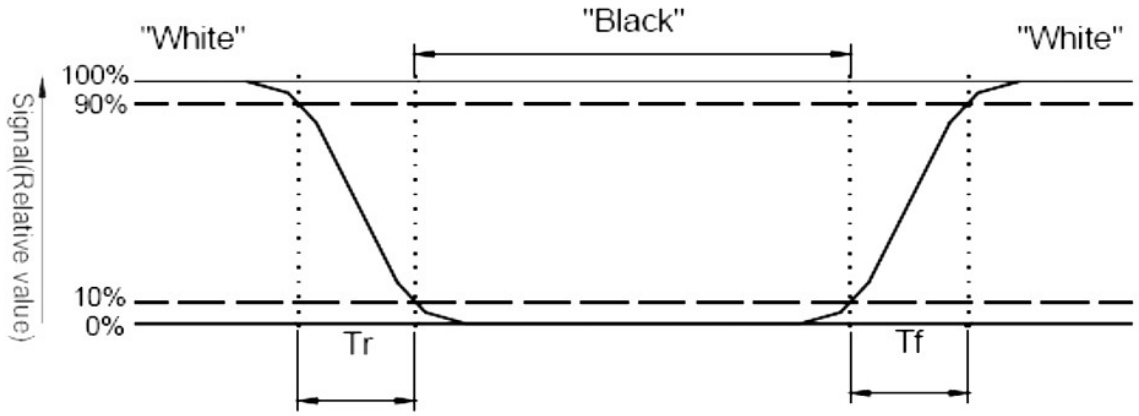
Item		Symbol	Condition	Values			Unit	Remark
				Min.	Typ.	Max.		
Viewing Angle Range	Left	θ_L	CR≧10	75	80	-	degree	Note 1
	Right	θ_R		75	80	-		
	Top	Φ_T		75	80	-		
	Botto	Φ_B		75	80	-		
Response Time		T_{on} +T_{off}	Normal θ=Φ=0˚	-	30	35	ms	Note 2
Contrast Ratio		CR	Normal θ=Φ=0˚	1000	1200	-	-	Note 3
Color Chromaticity (CF only with C light, CIE 1931)		Rx	Normal θ=Φ=0˚	0.572	0.622	0.672		Note5
		Ry		0.285	0.335	0.385		
		Gx		0.261	0.311	0.361		
		Gy		0.552	0.602	0.652		
		Bx		0.095	0.145	0.195		
		By		0.01	0.04	0.09		
		Wx		0.226	0.276	0.326		
		Wy		0.242	0.292	0.342		
Color Gamut (CF only with C light, CIE 1931)		NTSC	θ= 0°, Φ=0° CIE1931	65%	70%	-	%	
Luminance		L	Normal θ=Φ=0˚	200	250	-	cd/m2	Note 4

Note 1: Definition of viewing angle range



Note 2: Definition of response time

The response time is defined as the LCD optical switching time interval between “White” state and “Black” state. Rise time (T_{on}) is the time between photo detector output intensity changed from 90% to 10%, and fall time (T_{off}) is the time between photo detector output intensity changed from 10% to 90%.



Note 3: Definition of contrast ratio

Contrast ratio is calculated by the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Brightness on the "white" state}}{\text{Brightness on the "black" state}}$$

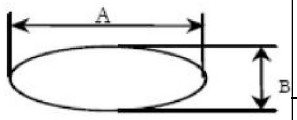
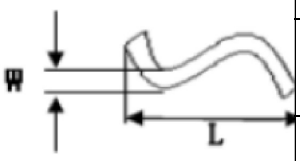
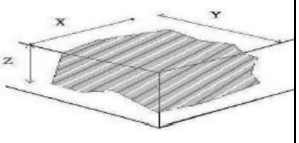
Note 4: Definition of luminance

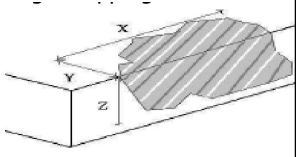
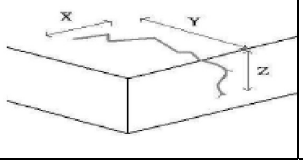
Measured at the center area of the panel when LCD panel is driven at “white” state.

Note 5: Definition of color chromaticity (CIE1931)

Color coordinates measured at the center point of LCD when panel is driven at “White”, “Red”, “Green” and “Blue” state respectively.

6.THE STANDARD OF INSPECTION

Item NO.	Inspection Item	Inspection Standard		Classification of defects
1	LCD Electrical function testing	1) No display 2) Missing line 3) No backlight 4) shadow 5) black/blue display 6) Irregular operating 7) visual angle is wrong		Major
2	CTP function test	No open and No short for ALL X/Y sensors, test of accuracy/linearity/sensitivity/separation/ Jitter/anti-moisture is OK		Major
3	Outline dimension	All outline dimension beyond the drawing is not allowed		Major
4	White/Black spot (in LCD or Backlight)  D=(A+B)/2	D≤0.10mm	Ignore.	Minor
		0.10mm<D≤0.25mm	To be max 3points. (distance≥5mm)	
		D>0.25mm	Not allowed.	
5	Color/bright/dark dot	Color not allowed Bright/dark dot as same as White/Black spot		Minor
6	Dirt in CTP	as same as White/Black spot		Minor
7	Dent at CTP	as same as White/Black spot		Minor
8	Bubble	as same as White/Black spot		Minor
9	Scratch /Lines defect:  	W≤0.02mm,L≤5mm	Ignore.	Minor
		0.02mm<W≤0.05mm; L≤5.00mm	N≤3（distance≥10mm）	
		W>0.05mm，L＞5mm	Not allowed.	
10	Particle lines defect	W≤0.02mm,L≤2.5mm	Ignore.	Minor
		0.02mm<W≤0.05mm; L≤2.50mm	N≤2（distance≥10mm）	
		W>0.05mm，L＞2.5mm	Not allowed.	
11	Conner Chipping:  	Length X<1.0 mm Width Y<1.0mm Thickness Z ≤ Glass thickness (Sealant area could not be broken)		Minor

12	Edge Chipping:  	Length X<1.5 mm Width Y<1.5 mm Thickness Z ≤ Glass thickness (Sealant area could not be broken)	Minor
13	Crack:  	Not allowed.	Minor

Note: 1. Viewing distance: 30 +/- 2 cm

2. Inspection angle: 45 degrees in 6 o’ clock direction (all defects in viewing area should be inspected from this direction),Rotate 30° about the vertical axis.

3. Light Source: 500~700Lux +/- 20%, black background.

7.RELIABILITY TESTS

ITEM	CONDITION	CRITERION
Operating Temperature Test	High Temperature: +70 ºC, 240 hrs	No defects in display and operational functions
	Low Temperature: -20 ºC,240 hrs	
Storage Temperature Test	High Temperature: +80 ºC, 240 hrs	No defects in display and operational functions
	Low Temperature: -30 ºC, 240 hrs	
Humidity Endurance Test	60ºC, 90%RH, 240 hrs	No defects in display and operational functions
Thermal Shock Test	-20 ºC (30mins)～ +70 ºC (30mins) 100 cycles	No defects in display and operational functions

NOTE:

1) The samples must be free from defect before test, must be restored at room condition at least for 2 hours after reliability test before any inspection.

2) Before test the function of TP, the sample must be placed in room temperature for 24hrs after RA test.

8. PRECAUTIONS

8.1. Handling

9.1.1. Polarizer Cleaning, Petroleum ether (or N-hexane) is recommended for cleaning the front/rear polarizers and reflectors, acetone, toluene and ethanol are not allowed to avoid damaging the surface.

9.1.2. Body grounding, must wear Anti-ESD wrist strap while pick up LCDs.

9.1.3. FPC Soldering, less than 300℃/3S, solder must be grounding on grounding bench.

9.1.4. If use electric Screwdriver to do assembly, screwdriver must be grounding.

8.2. Storage

9.2.1. Keep in a sealed polyethylene bag.

9.2.2. Keep in a dark place.

9.2.3. Keep in temperature between 0ºC and 35ºC.

NOT allowed at 70ºC for more than 160 Hours, or at -20ºC for more than 48 Hrs.

8.3. Safety

If liquid crystal leak out of a damaged glass cell, DO NOT put it in your mouth or touch eyes, if the liquid crystal touch your skin or clothes, please wash it off immediately using soap and water.

9. LIMITED WARRANTY

Unless otherwise agreed between IIDWay and customer, IIDWay will replace or repair any of its LCD modules which are found to be functionally defective when inspected in accordance with IIDWay LCD acceptance standards (copies available upon request) for a period of one year from date of shipments. Cosmetic/visual defects over specs must be returned to IIDWay within 30 days of shipment. Confirmation of such date shall be based on freight documents. The warranty liability of IIDWay limited to repair and/or replacement on the terms set forth above. IIDWay shall not be responsible for any subsequent or consequential events.

9.1. Returning Lcm Under Warranty – Terms And Conditions

10.1.1. No warranty can be granted if the precautions stated above have been disregarded. The typical examples of violations are :

- Broken LCD glass.
- Circuit modified in any way, including addition of components.

10.1.2. Module repairs will be invoiced to the customer upon mutual agreement. Modules must be returned with sufficient description of the failures or defects. Any connectors or cable installed by the customer must be removed completely without damaging the PCB’s eyelet, conductors and terminals.