REV	00

IIDWAY TECHNOLOGY CO.,LTD

样 品 承 认 书

APPROVAL SHEET

PRODUCT MODEL	GZ70206-PIT069TH		
REMARKS	TFT MODULE, 480 (RGB) *1280PIXELS		
APPROVED SIGNATURE BY CUSTOMER	PROJECT	QUALITY	APPROVED

PREPARED BY	CHECKED BY	APPROVED BY

RECORDS OF REVISION

REV.	DATE	PAGE	DESCRIPTION OF CHANGES
00	2022.10.12		First issue.

CONTENT

1. GENERAL SPECIFICATION

1.1 Description

The GZ70206-PIT069TH is a color active matrix Thin Film Transistor (TFT) Liquid Crystal Display (LCD) that uses amorphous silicon(a-Si) TFT as a switching device,and with a Capacitive Touch Panel(CTP). This model is composed of a single 6.67 inches transmissive type main TFT-LCD panel. The resolution of the panel is 480RGBx1280 pixels and can display up to 16.7M color.

1.2 Feature

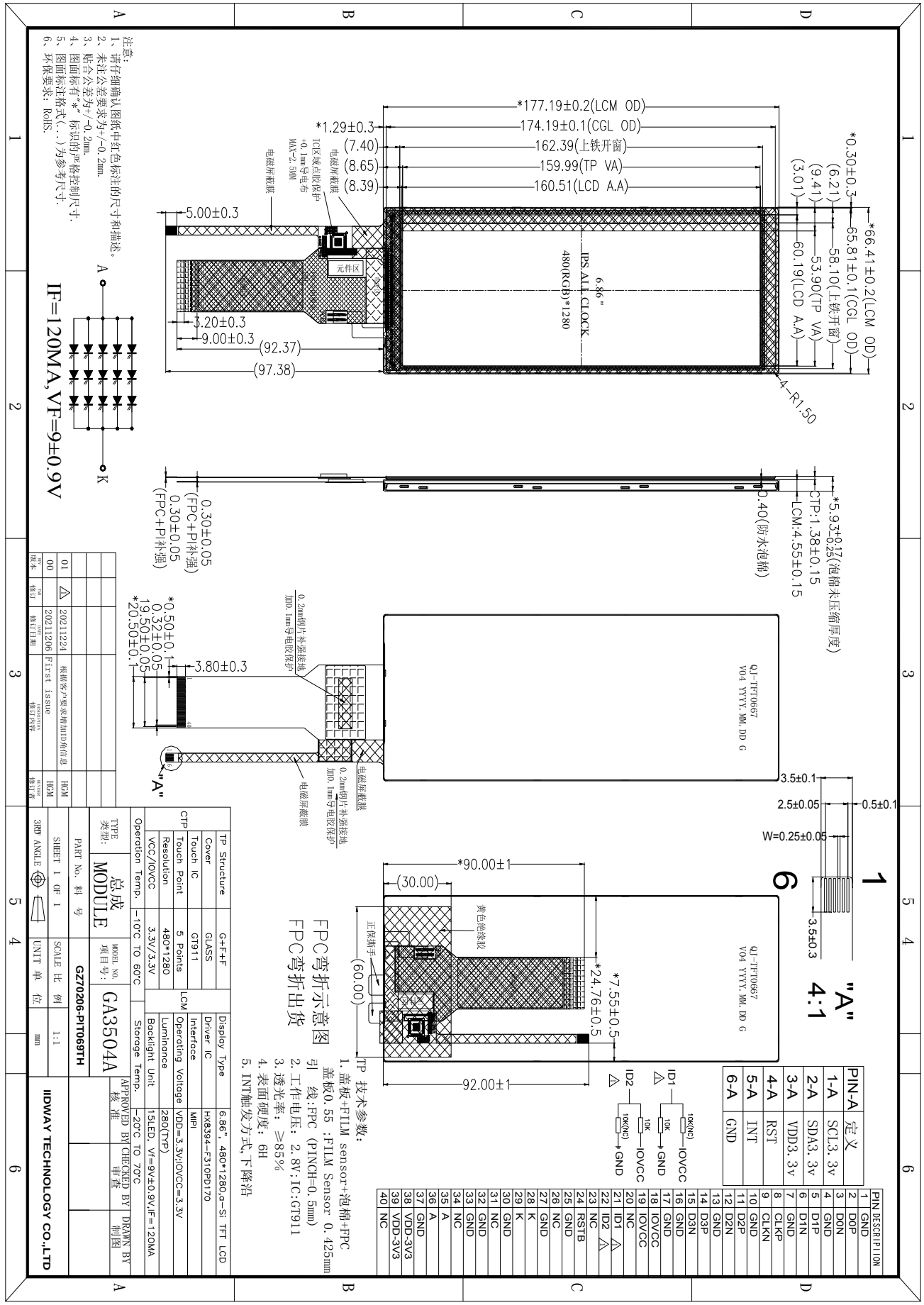
-IPS type for main TFT-LCD panel
-Structure COG+FPC+BL+CTP
-Full, Normal (Still), Partial, Sleep mode are available

1.3 General Specification

No.	Item	Specification	Unit	Remark
1	LCD Size	6.67	inch	-
2	Panel Type	a-Si TFT active matrix	-	-
3	Resolution	480 x (RGB) x 1280	pixel	-
4	Display Mode	Normally Black,Transmissive	-	-
5	Display Number of Colors	16.7M	-	-
6	Viewing Direction	Free	-	Note
7	Contrast Ratio	1000(MIN),1500(TYP)	-	-
8	Luminance	280(TYP)	cd/m^2	-
9	Module Size	66.41(W) x177.19(L) x5.93(T)	mm	Note
10	Active Area	60.19(W) x160.51(L)	mm	Note
11	Pixel Pitch	0.1254(W) x 0.1254（L）	mm	-
12	Driver IC	HX8394-F310PD170	-	-
13	Light Source	15 LEDs White	-	-
14	Interface	MIPI	-	-
15	Operating Temperature	-10~60	℃	-
16	Storage Temperature	-20~70	℃	-

Note: Please refer to the mechanical drawing.

2. MECHANICAL DRAWING



PIN-A	定义
1-A	SCL3. 3v
2-A	SDA3. 3v
3-A	VDD3. 3v
4-A	RST
5-A	INT
6-A	GND

PIN	DESCRIPTION
1	GND
2	D0P
3	D0N
4	GND
5	D1P
6	D1N
7	GND
8	CLKP
9	CLKN
10	GND
11	D2P
12	D2N
13	GND
14	D3P
15	D3N
16	GND
17	GND
18	IOVCC
19	IOVCC
20	NC
21	ID1 △
22	ID2 △
23	NC
24	RSTB
25	GND
26	NC
27	GND
28	K
29	K
30	GND
31	NC
32	GND
33	GND
34	NC
35	A
36	A
37	GND
38	VDD-3V3
39	VDD-3V3
40	NC

TP 技术参数:
1. 盖板+FILM sensor+泡棉+FPC
盖板0.55 ;FILM Sensor 0.425mm
引 线:FPC (PINCH=0.5mm)
2. 工作电压: 2.8V;IC:GT911
3. 透光率: ≥85%
4. 表面硬度: 6H
5. INT触发方式,下降沿

FPC弯折示意图
FPC弯折出货

注意:
1、请仔细确认图纸中红色标注的尺寸和描述。
2、未注公差要求为+/-0.2mm.
3、贴合公差为+/-0.2mm.
4、图面标有"*"标识的严格控制尺寸.
5、图面标注格式(...)为参考尺寸.
6、环保要求: RoHS.

版本 VER.	修订 REVISION	修订日期 DATE	修订内容 DESCRIPTION	修订者 REVISION BY
01	△	20211224	根据客户要求增加ID角信息	HGM
00		20211206	First issue	HGM

TP Structure	G+F+F	Display Type	6.86", 480*1280, a-Si TFT LCD
Cover	GLASS	Driver IC	HX8394-F310PD170
Touch IC	GT911	Interface	MIPI
Touch Point	5 Points	Operating Voltage	VDD=3.3V;IOVCC=3.3V
Resolution	480*1280	Luminance	280(TYP)
VCC/IOVCC	3.3V/3.3V	Backlight Unit	15LED, Vf=9V±0.9V,IF=120MA
Operation Temp.	-10°C TO 60°C	Storage Temp.	-20°C TO 70°C

CTP / LCM

TYPE 类型:	总成 MODULE	MODEL NO. 项目号:	GA3504A
PART No. 料 号			GZ70206-PIT069TH
SHEET 1 OF 1		SCALE 比 例	1:1
3RD ANGLE		UNIT 单 位	mm

APPROVED BY 核 准	CHECKED BY 审 查	DRAWN BY 制 图

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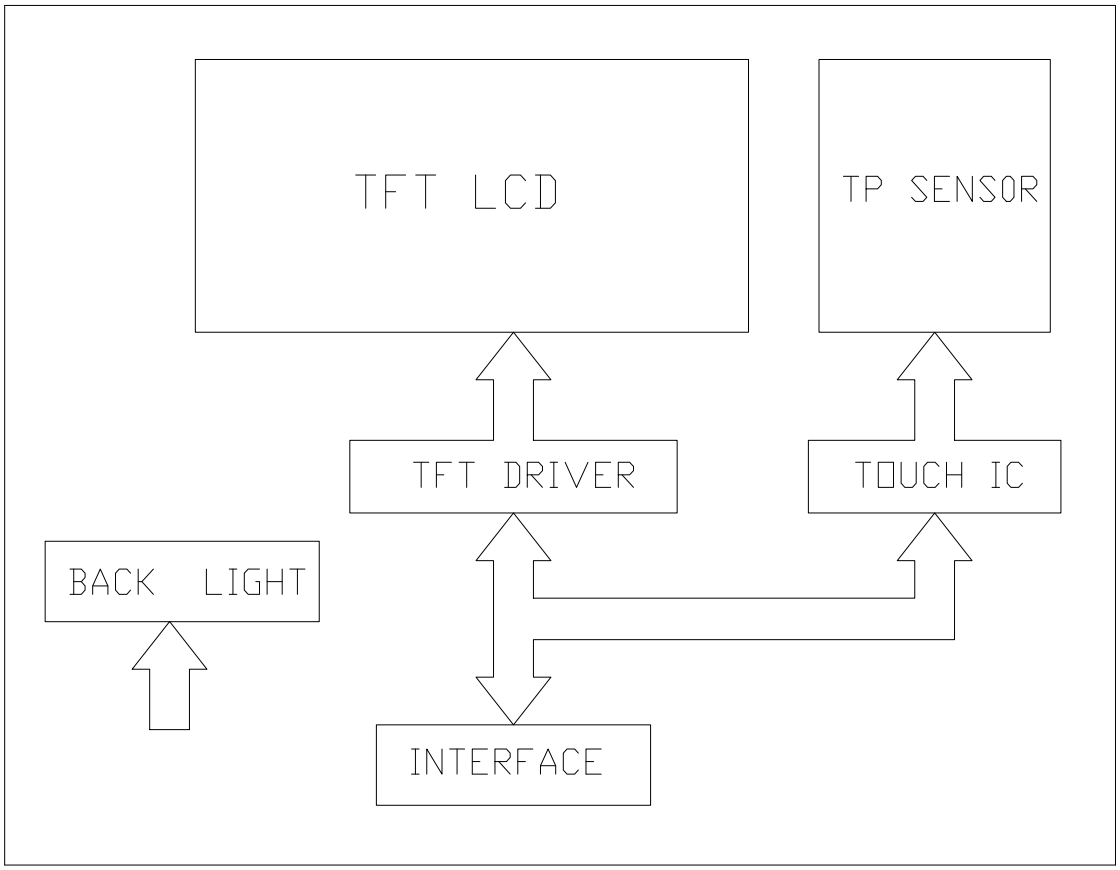
3. INTERFACE ASSIGNMENT

1	GND	Ground
2	D0P	MIPI-DSI Data differential signal input pins. (Data lane 0)
3	D0N	MIPI-DSI Data differential signal input pins. (Data lane 0)
4	GND	Ground
5	D1P	MIPI-DSI Data differential signal input pins. (Data lane 1)
6	D1N	MIPI-DSI Data differential signal input pins. (Data lane 1)
7	GND	Ground
8	CLKP	MIPI-DSI CLOCK differential signal input pins.
9	CLKN	MIPI-DSI CLOCK differential signal input pins.
10	GND	Ground
11	D2P	MIPI-DSI Data differential signal input pins. (Data lane 2)
12	D2N	MIPI-DSI Data differential signal input pins. (Data lane 2)
13	GND	Ground
14	D3P	MIPI-DSI Data differential signal input pins. (Data lane 3)
15	D3N	MIPI-DSI Data differential signal input pins. (Data lane 3)
16	GND	Ground
17	GND	Ground
18	IOVCC	A power supply for the logic power and I/O circuit.
19	IOVCC	A power supply for the logic power and I/O circuit.
20	NC	No connection
21	ID1	LCM Identify
22	ID2	LCM Identify
23	NC	No connection
24	RSTB	Global reset pin
25	GND	Ground
26	NC	No connection
27	GND	Ground
28	K	Cathode power supply for backlight (LED-).
29	K	Cathode power supply for backlight (LED-).
30	GND	Ground
31	NC	No connection
32	GND	Ground
33	GND	Ground
34	NC	No connection
35	A	Anode power supply for backlight (LED+).
36	A	Anode power supply for backlight (LED+).
37	GND	Ground
38	VDD-3V3	Power supply for digital circuits 3.3V
39	VDD-3V3	Power supply for digital circuits 3.3V
40	NC	No connection

4. ELECTRICAL SPECIFICATION

4.1. Block Diagram



4.2. Tft Absolute Maximum Ratings

ITEM	SYMBOL	CONDITION	STANDARD VALUE			UNIT
			MIN	TYP	MAX	
Power Supply for Digital IO	IOVCC	Ta=25 ºC	-0.3	-	3.6	V
Analog Operating Voltage	VDD	Ta=25 ºC	-0.3		3.6	

Note: Permanent damage to the device may occur if maximum values are exceeded or reverse voltage is applied.

4.3. Tft Typical Operation Condition

4.3.1 TFT DC Characteristics

ITEM	SYMBOL	CONDITION	STANDARD VALUE			UNIT
			MIN	TYP	MAX	
Power Supply for Digital IO	IOVCC	Ta=25 ºC	1.65	3.3	3.6	V
Analog operating voitage	VDD	Ta=25 ºC	2.5	3.3	3.6	V
Input Signal “H” Level	V_{IH}	-	0.7IOVCC	-	IOVCC	V
Input Signal “L” Level	V_{IL}	-	0	-	0.3IOVCC	V
Output Signal “H” Level	V_{OH}	I_{OH}=-1.0mA	0.8IOVCC	-	IOVCC	V
Output Signal “L” Level	V_{OL}	I_{OL}=1.0mA	0	-	0.2IOVCC	V
Frame Frequency	FRAME	-	-	60	-	Hz

Note: To prevent IC latch up or DC operation in LCD panel, the power on/off sequence should follow the driver IC specification.

4.3.2 TFT Current Consumption

Item	Symbol	Values		Unit	Remark
		type	Max.		
MIPI 4-Lane Interface					
Normal(Still) Mode	I_{VCC}	60	90	mA	Note1
Standby Mode	I_{VCC}	20	100	uA	Note2

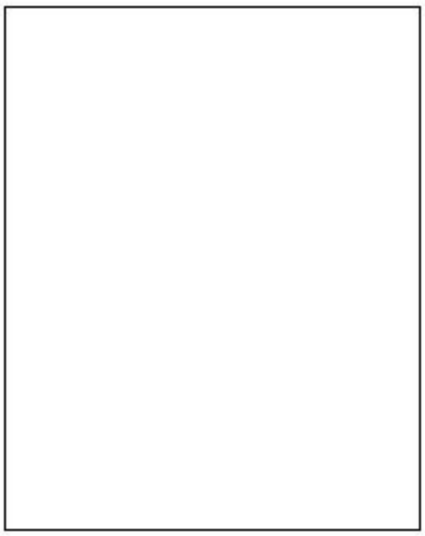
Note1: Test Condition

Typ: IOVCC=3.3V,VDD=3.3V

Display Pattern: All Pixel White

Frame Rate=60Hz at Column Inversion

Max. current check pattern:

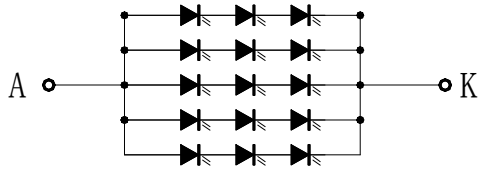


White

Note2: In the standby mode, all the internal display operations are suspended including the internal R-C oscillator.

4.4. Backlight Specification

4.4.1 Backlight Circuit



IF=120MA,VF=9±0.9V

4.4.2 ELECTRICAL CHARACTERISTICS **(T=25℃)**

PARAMETER	SYMBOL	CONDITION	STANDARD VALUE			UNIT
			MIN	TYP	MAX	
FORWARD VOLTAGE	VF	IF=120mA	8.1	9	9.9	V

4.5 Power on/off Timing:

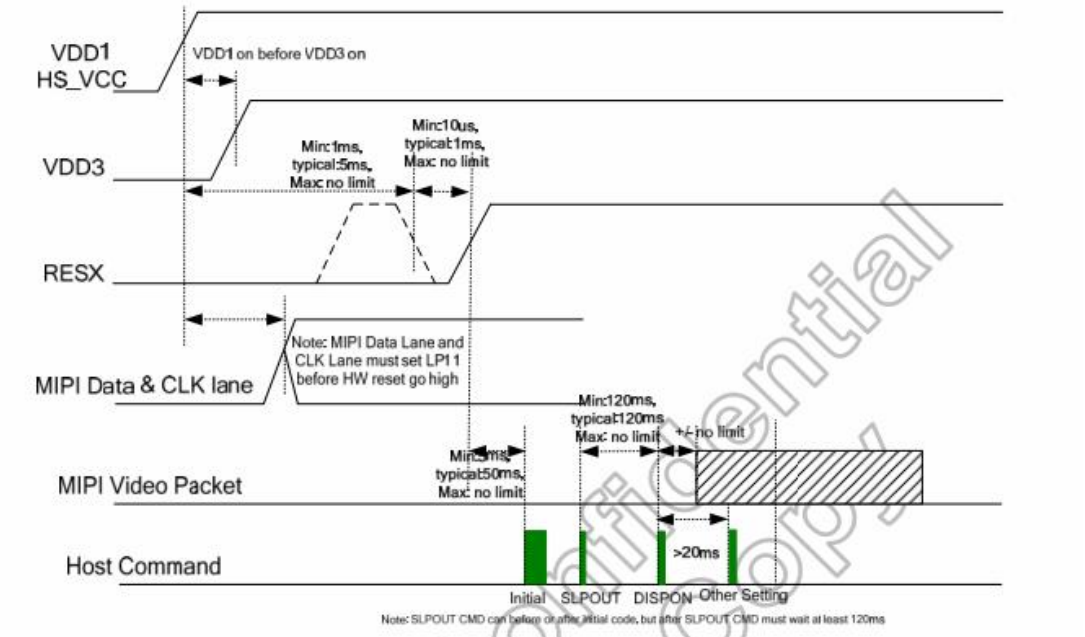


Figure 5.28: VDD1/VDD3 input power on sequence

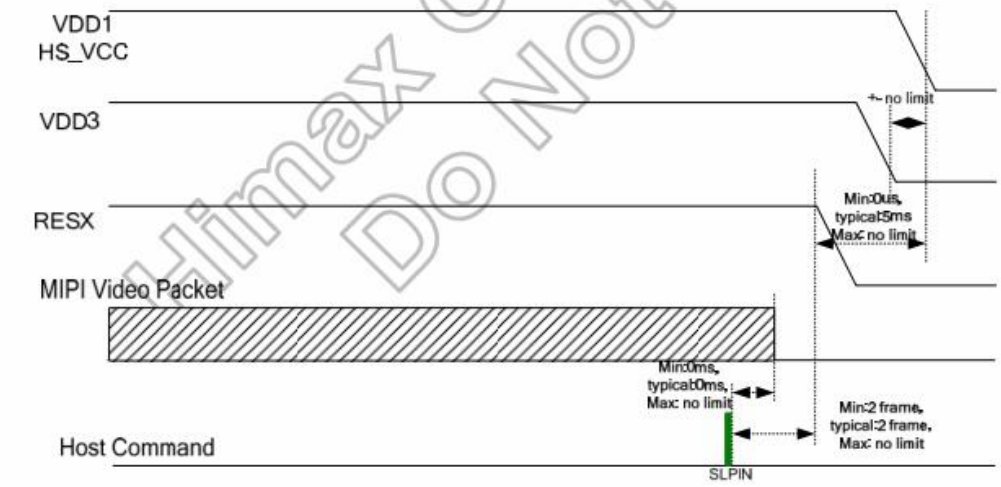


Figure 5.29: VDD1/VDD3 input power off sequence

4.6.Interface Characteristics:

High speed data transmission

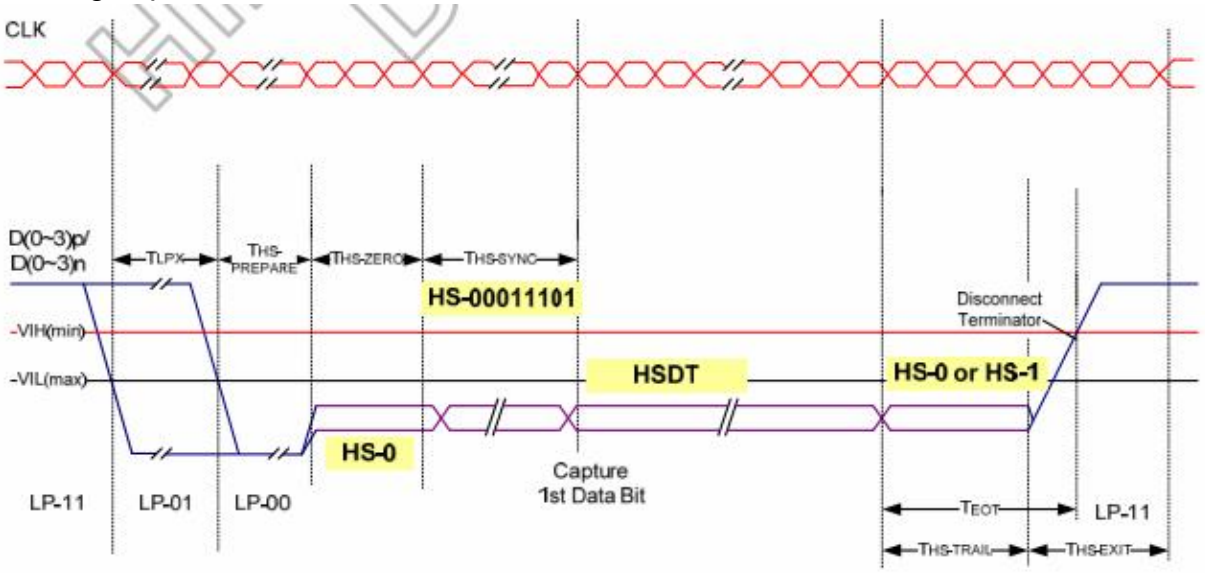


Figure 4.12: High speed data transmission timing sequence

Parameter	Description	Spec.			Unit
		Min.	Typ.	Max.	
$T_{HS-PREPARE}$	Time that the transmitter drives the Data Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission.	40+4*UI	-	85+6*UI	ns
$T_{HS-PREPARE}$+ $T_{HS-ZERO}$	THS-PREPARE + time that the transmitter drives the HS-0 state prior to transmitting the Sync sequence.	145+10*UI	-	-	ns
T_{EOT}	Transmitted time interval from the start of THS-TRAIL or TCLK-TRAIL, to the start of the LP-11 state following a HS burst.	-	-	105ns+12*UI	ns
$T_{HS-TRAIL}$	Time that the transmitter drives the flipped differential state after last payload data bit of a HS transmission burst.	60ns+4*UI	-	-	ns
$T_{HS-EXIT}$	Time that the transmitter drives LP-11 following a HS burst.	100	-	-	ns

Table 4.2: Global operation timing parameters for data lane

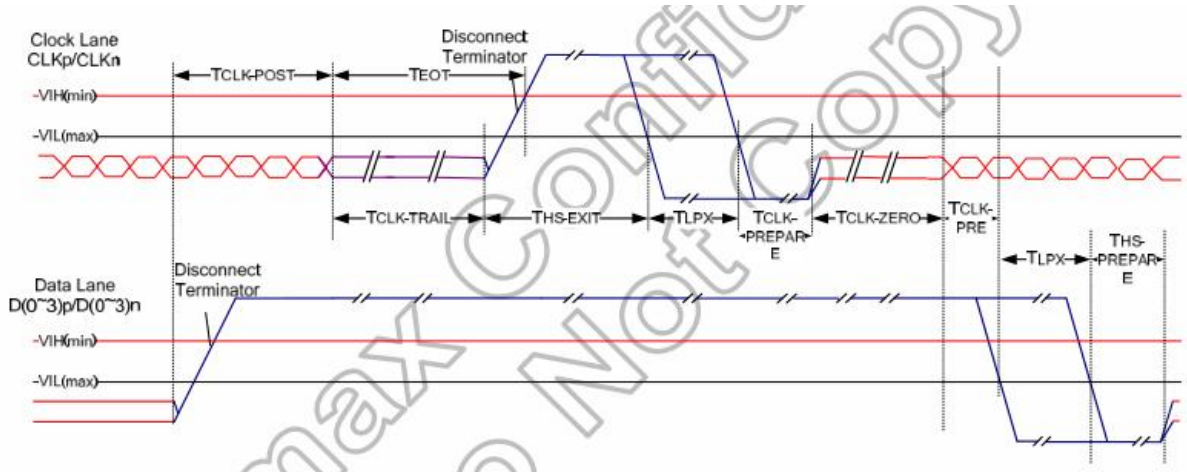


Figure 4.13: Switching the clock lane between clock transmission and LP mode

Parameter	Description	Spec.			Unit
		Min.	Typ.	Max.	
$T_{CLK-POST}$	Time that the transmitter continues to send HS clock after the last associated Data Lane has transitioned to LP Mode.	60+52*UI	-	-	ns
$T_{CLK-TRAIL}$	Time that the transmitter drives the flipped differential state after last payload data bit of a HS transmission burst.	60	-	-	ns
$T_{CLK-PREPARE}$	Time that the HS clock shall be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode.	38	-	95	ns
$T_{CLK-PREPARE+}$ $T_{CLK-ZERO}$	TCLK-PREPARE + time that the transmitter drives the HS-0 state prior to starting the Clock.	300	-	-	ns
$T_{CLK-PRE}$	Time that the HS clock shall be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode.	8*UI	-	-	ns

Table 4.3: Global operation timing parameters for clock lane

5. TOUCH PANEL SPECIFICATION

5.1. General Specification

No.	Item	Specification	Unit
1	Size	6.67	inch
2	Type	Capacitive Touch Panel	-
3	Touch Panel Structure	Glass Cover+Film Sensor	-
4	Touch Panel Surface Hardness	≥6H	-
5	Transmittance	≥85	%
6	Touch Panel Controller IC	GT911	-
7	Touch Panel Interface	I2C	-

5.2. FPC PIN Assignment

PIN NO.	SYMBOL	FUNCTION DESCRIPTIONS
1	SCL3.3V	I2C Serial clock input/output
2	SDA3.3V	I2C Serial data input/output
3	VDD3.3V	POWER supply for system
4	RST	Reset signal
5	INT	External Interrupt
6	GND	Ground

5.3.DC Characteristics

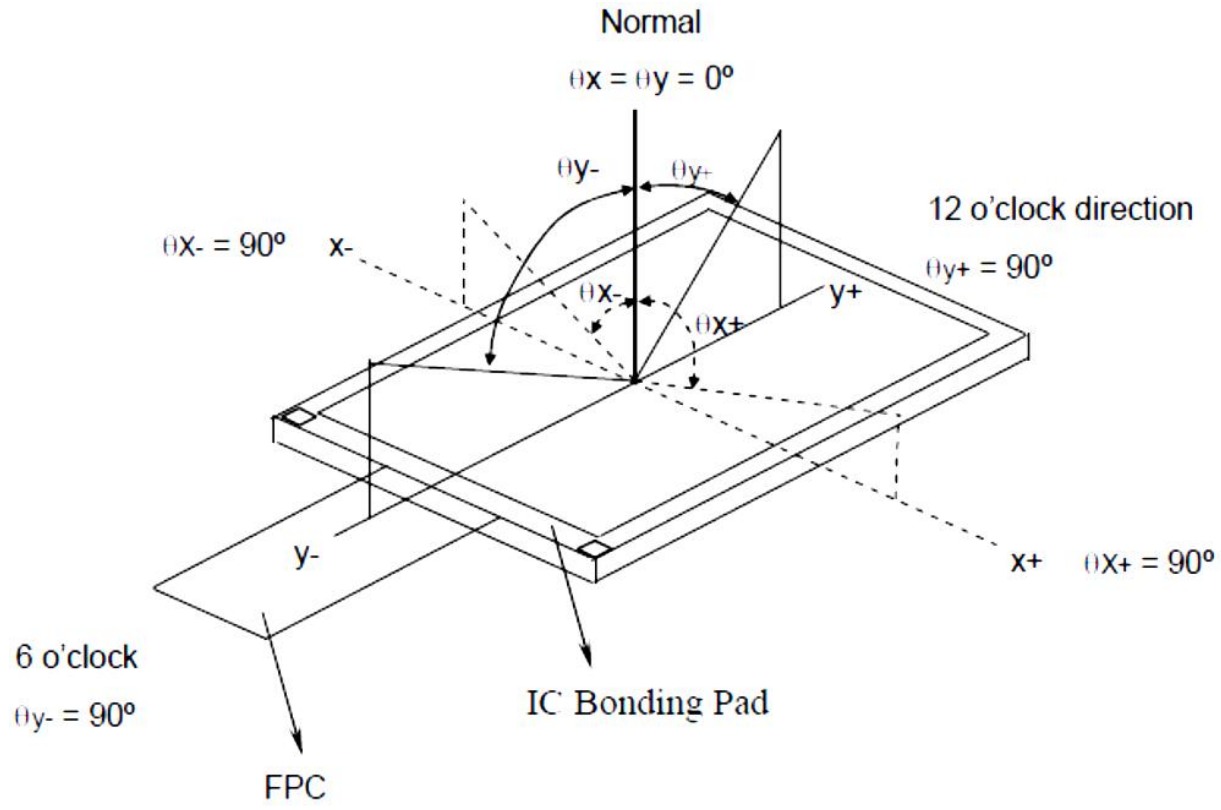
ITEM	SYMBOL	CONDITION	STANDARD VALUE			UNIT
			MIN	TYP	MAX	
Power Supply for Analog	VDD	Ta=25 ºC	-	3.3	-	V
Power Supply for Digital IO	IOVDD	Ta=25 ºC	-	3.3	-	V
Input Signal “H” Level	VIH	IOVDD=3.3V	0.75*IOVDD	-	IOVDD+0.3	V
Input Signal “L” Level	VIL		-0.3	-	0.3*IOVDD	V

6. LCD OPTICAL CHARACTERISTICS

(T_a=+25ºC, VDD=+3.3V IOVCC=+3.3V)

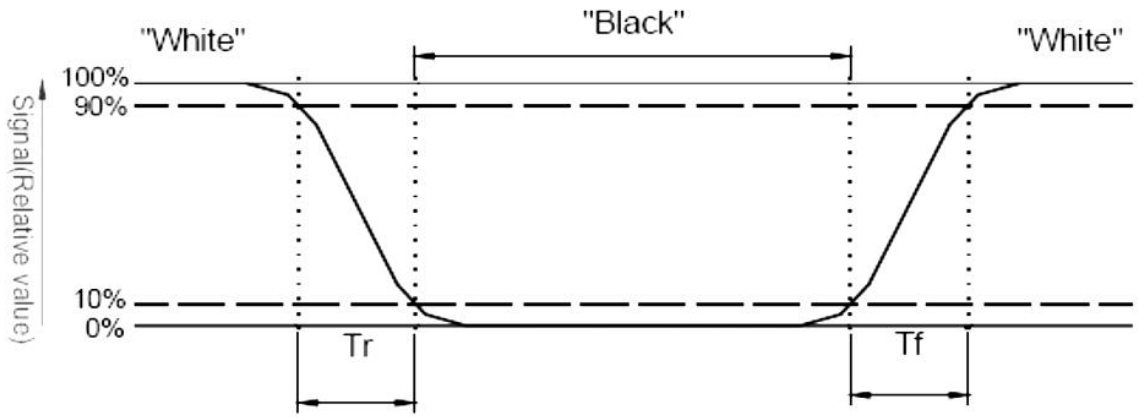
Item		Symbol	Condition	Values			Unit	Remark
				Min.	Typ.	Max.		
Viewing Angle Range	Left	θ_L	CR≧10	75	85	-	degree	Note 1
	Right	θ_R		75	85	-		
	Top	Φ_T		75	85	-		
	Botto	Φ_B		75	85	-		
Response Time		T_{on} +T_{off}	Normal θ=Φ=0˚	-	30	40	ms	Note 2
Contrast Ratio		CR	Normal θ=Φ=0˚	1000	1500	-	-	Note 3
Luminance		L	Normal θ=Φ=0˚	230	280	-	cd/m^2	Note 4
Color Chromaticity (CIE1931)	White	X	Normal θ=Φ=0˚	-0.03	0.27	+0.03	-	Note 5
		Y			0.28			

Note 1: Definition of viewing angle range



Note 2: Definition of response time

The response time is defined as the LCD optical switching time interval between "White" state and "Black" state. Rise time (T_{on}) is the time between photo detector output intensity changed from 90% to 10%, and fall time (T_{off}) is the time between photo detector output intensity changed from 10% to 90%.



Note 3: Definition of contrast ratio

Contrast ratio is calculated by the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Brightness on the "white" state}}{\text{Brightness on the "black" state}}$$

Note 4: Definition of luminance

Measured at the center area of the panel when LCD panel is driven at “white” state.

Note 5: Definition of color chromaticity (CIE1931)

Color coordinates measured at the center point of LCD when panel is driven at “White”, “Red”, “Green” and “Blue” state respectively.

7.THE STANDARD OF INSPECTION

检验项目	检验标准	检测工具	缺陷等级
凹凸坑/异色点/白点	①.0.15mm＜D≤0.3mm，（S≤0.05mm² ）J≥10mm，N≤3，明显、亮点不可； ②.J≥10mm，D≤0.15mm 忽略不计，但不可密集（10mm 区域内 N≥2为密集）	目视、点规卡、卡尺	Min
透光	B 区：0.15mm＜D≤0.25mm，N≤2，J≥20mm D＞0.30mm 不允许	目视、点规卡、卡尺	Min
软划伤	全区域：（W：宽度，L：长度，N：个数，）W≤0.05mm，不限，J≥2mm；W≤0.1mm，L≤5mm，N≤1；W≤0.08mm；L≤5mm N≤2;W＞0.2mm，L＞5mm 不允许	目视、点规卡、卡尺	Min
硬划伤	可视区不可以，其他区域允许	目视、点规卡、卡尺	Min
气泡/污斑	D＜0.3㎜（S＜0.13㎜²） 且 N＜2	目视、点规卡、卡尺	Min
脏污	可擦脏污允许	目视、点规卡、卡尺	MAJ
崩角/边	可视区不可见，不影响产品功能	目视、点规卡、卡尺	MAJ

裂痕/纹	不允许	目视、点规卡、卡尺	MAJ
手印	不允许	目视	MAJ
TP 牛顿环	小于 TP 面积的 1/6	目视、点规卡、卡尺	MAJ
漏光	不允许	目视、点规卡、卡尺	MAJ
背胶粘性不良	不允许	目视、点规卡、卡尺	MAJ
显示屏黑线/残影/花屏	不允许	目视、点规卡、卡尺	MAJ
显示屏黑点	0mm＜D≤0.15mm, J≥10mm，N≤3,（10mm 区域内 N≥2 为密集），黑点不可在界面白色区域	目视、点规卡、卡尺	MAJ
颜色	与标准样板（或颜色上下限度样板）符合	目视、点规卡、卡尺	MAJ

偏位	ITO Film与 lens 断差≤0.2mm 与配件（面壳）实配无影响	目视、点规卡、卡尺	MAJ
FPC	金手指断（裂）、折痕、分层、氧化、破损、露铜、少元件不允许	目视、点规卡、卡尺	MAJ

8.RELIABILITY TESTS

ITEM	CONDITION	CRITERION
Operating Temperature Test	High Temperature: +60 ºC, 240 hrs	No defects in display and operational functions
	Low Temperature: -10 ºC,240 hrs	
Storage Temperature Test	High Temperature: +70 ºC, 240 hrs	No defects in display and operational functions
	Low Temperature: -10 ºC, 240 hrs	
Humidity Endurance Test	40ºC, 90%RH, 240 hrs	No defects in display and operational functions
Thermal Shock Test	-20 ºC (30mins)～ +70 ºC (30mins) 10 cycles	No defects in display and operational functions
Electro Static Discharge	± 4KV, Human BodyMode,150pF/330Ω; ± 8KV,Air Mode,150pF/330Ω	No defects in display and operational functions

NOTE:

1) The samples must be free from defect before test, must be restored at room condition at least for 2 hours after reliability test before any inspection.

2) Before test the function of TP, the sample must be placed in room temperature for 24hrs after RA test.

9. PRECAUTIONS

9.1. Handling

9.1.1. Polarizer Cleaning, Petroleum ether (or N-hexane) is recommended for cleaning the front/rear polarizers and reflectors, acetone, toluene and ethanol are not allowed to avoid damaging the surface.

9.1.2. Body grounding, must wear Anti-ESD wrist strap while pick up LCDs.

9.1.3. FPC Soldering, less than 300℃/3S, solder must be grounding on grounding bench.

9.1.4. If use electric Screwdriver to do assembly, screwdriver must be grounding.

9.2. Storage

9.2.1. Keep in a sealed polyethylene bag.

9.2.2. Keep in a dark place.

9.2.3. Keep in temperature between 0ºC and 35ºC.

NOT allowed at 70ºC for more than 160 Hours, or at -20ºC for more than 48 Hrs.

9.3. Safety

If liquid crystal leak out of a damaged glass cell, DO NOT put it in your mouth or touch eyes, if the liquid crystal touch your skin or clothes, please wash it off immediately using soap and water.

10. LIMITED WARRANTY

Unless otherwise agreed between SUPERVIEW and customer, SUPERVIEW will replace or repair any of its LCD modules which are found to be functionally defective when inspected in accordance with SUPERVIEW LCD acceptance standards (copies available upon request) for a period of one year from date of shipments. Cosmetic/visual defects over specs must be returned to SUPERVIEW within 30 days of shipment. Confirmation of such date shall be based on freight documents. The warranty liability of SUPERVIEW limited to repair and/or replacement on the terms set forth above. SUPERVIEW shall not be responsible for any subsequent or consequential events.

10.1. Returning Lcm Under Warranty – Terms And Conditions

10.1.1. No warranty can be granted if the precautions stated above have been disregarded. The typical examples of violations are :

- Broken LCD glass.
- Circuit modified in any way, including addition of components.

10.1.2. Module repairs will be invoiced to the customer upon mutual agreement. Modules must be returned with sufficient description of the failures or defects. Any connectors or cable installed by the customer must be removed completely without damaging the PCB’s eyelet, conductors and terminals.